LIBRARY ieee ;

USE ieee.std\_logic\_1164.all ;

USE ieee.std\_logic\_signed.all ;

ENTITY lab6c IS

PORT ( add\_sub : IN STD\_LOGIC;

A, B : IN STD\_LOGIC\_VECTOR(3 DOWNTO 0) ;

Result : OUT STD\_LOGIC\_VECTOR(3 DOWNTO 0) ;

Parity\_Flag : OUT STD\_LOGIC;

Carry\_Flag : OUT STD\_LOGIC ;

Overflow : OUT STD\_LOGIC ) ;

END lab6c ;

ARCHITECTURE Behavior OF lab6c IS

BEGIN

Process(A,B,add\_sub)

VARIABLE temp: STD\_LOGIC\_VECTOR (4 DOWNTO 0);

Begin

IF(add\_sub = '1') THEN

temp := ('0' & A) - ('0' & B);

ELSE

temp := ('0' & A) - ('0' & B);

END IF;

Result <= temp(3 DOWNTO 0);

Carry\_Flag <= temp(4);

Overflow <= A(3) XOR B(3) XOR temp(3) XOR temp(4);

END Process;

Process (A,B)

VARIABLE temp: STD\_LOGIC;

Begin

temp := A(0) XOR B(0);

IF(temp = '1') THEN

Parity\_Flag <= '1';

ELSE

Parity\_Flag <= '0';

END IF;

END Process;

END Behavior ;